Transitioning eMRAM from Pilot Project to Volume Production

2023 International Test Conference

arm

SIEMENS

Purpose

- Supporting eMRAM technology in a high-volume production environment requires:
  - automation to optimize the DFT implementation
  - integrated ECC and repair capabilities to improve yield and durability

Outline

- Introduction to MRAM, industry landscape
- MRAM testing challenges
  - ECC-aware Test and Repair technology
  - Automated Read self-trimming
- Summary and Conclusion

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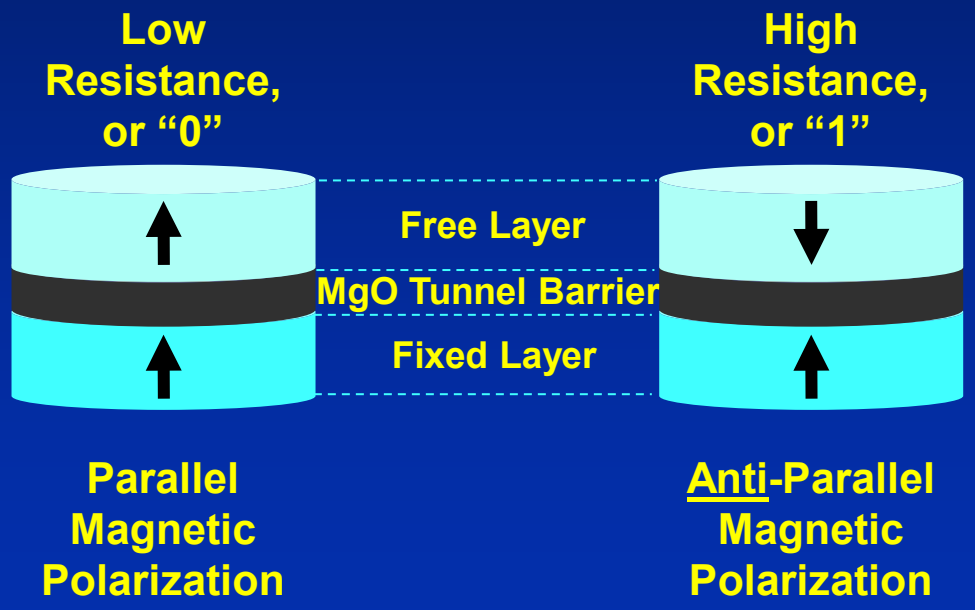
What is (STT-) MRAM?

CMOS-friendly, fast, dense and low mask adder non-volatile memory

- MRAM stands for *Magneto-resistive RAM*
  Magnetic polarization sets the memory state
- STT stands for *Spin Transfer Torque*
  Electron spin is used to switch magnetic polarization
- 1T-1MTJ bitcell
  Allows dense configuration and scalability
  MTJ in metal stack enables low mask count add

Memory element Perpendicular Magnetic Tunnel Junction (pMTJ)



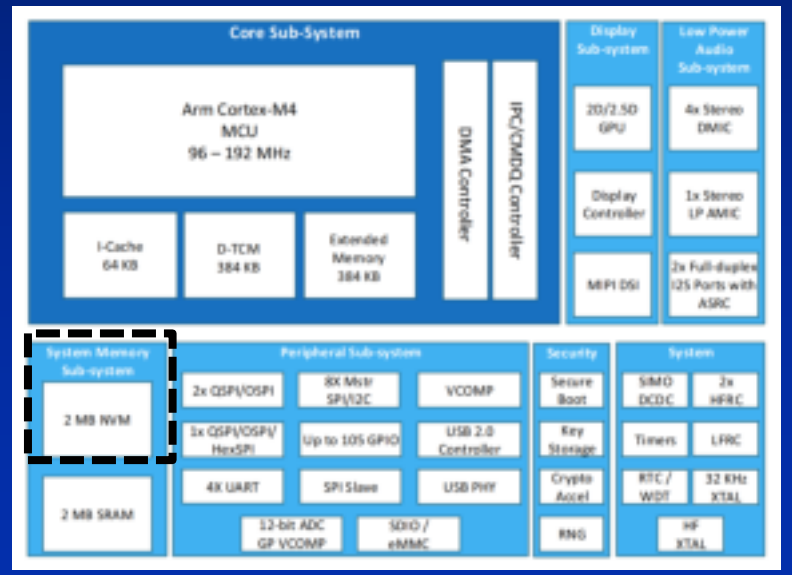
Current industry landscape

Wearables, fusion processors & microcontrollers, AI/ML acceleration

Ambiq Apollo 4 SoCs

2MB 22nm MRAM

Arm® Cortex®-M4F core

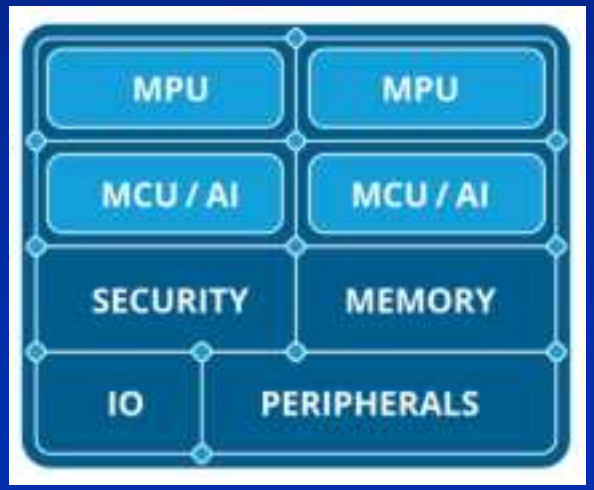


Alif Semiconductor Ensemble™ Family

Up to 5.5MB MRAM

Arm® Cortex®-M55, A32

Arm Ethos™-U55 microNPUs for AI/ML acceleration



Sony Semiconductor Solutions

GPS/GNSS receiver/processor chips

2MB 28nm MRAM

Built-in SONY CXD5605 low-power chip, support GPS, Beidou, qzss global satellite positioning system, with intelligent mileage optimization algorithm, more accurately improve the motion trajectory and mileage accuracy, and record motion data more accurately
SONY low consumption chip
GPS
qZss positioning
Beidou
08
30
Found in Huawei smartwatch GT 2

Arm and Siemens EDA MRAM collaboration

- Arm collaborated with Siemens EDA to develop an automated solution for handing embedded MRAM technology
  - Goal is to help bring a new industry standard testing solution to market
- Arm provides an MRAM compiler IP for Samsung 28nm FDSOI technology
  - IP was used as the basis to validate the new automated MBIST technology

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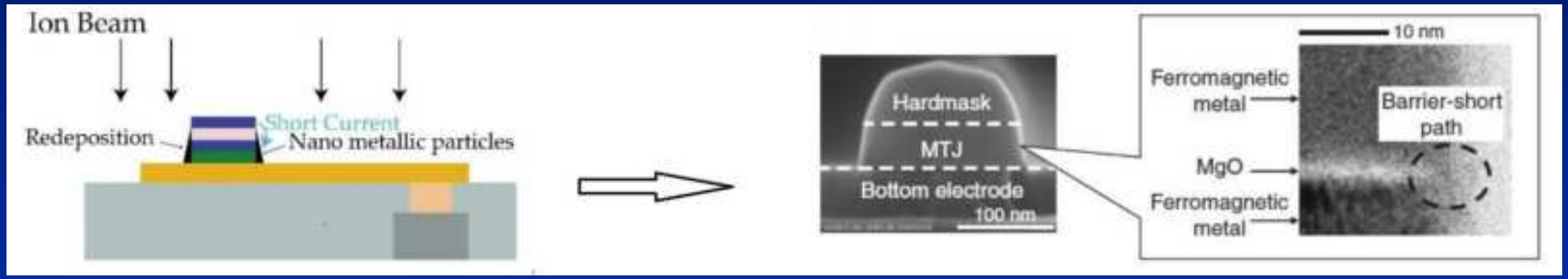
Why Error-Correcting Codes (ECC) for MRAM

- Write operation is stochastic in nature, so in-field failures can occur
- Some bit cells are defective upon manufacturing, and ECC is a better option to “repair” them instead of using spare elements

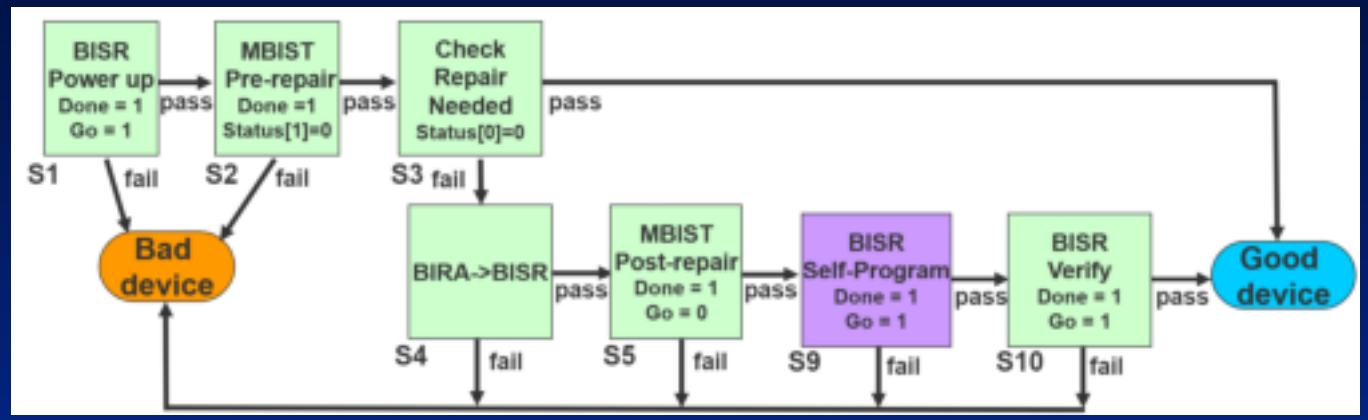


Source: A Survey on STT-MRAM Testing: Failure Mechanisms, Fault Models, and Tests

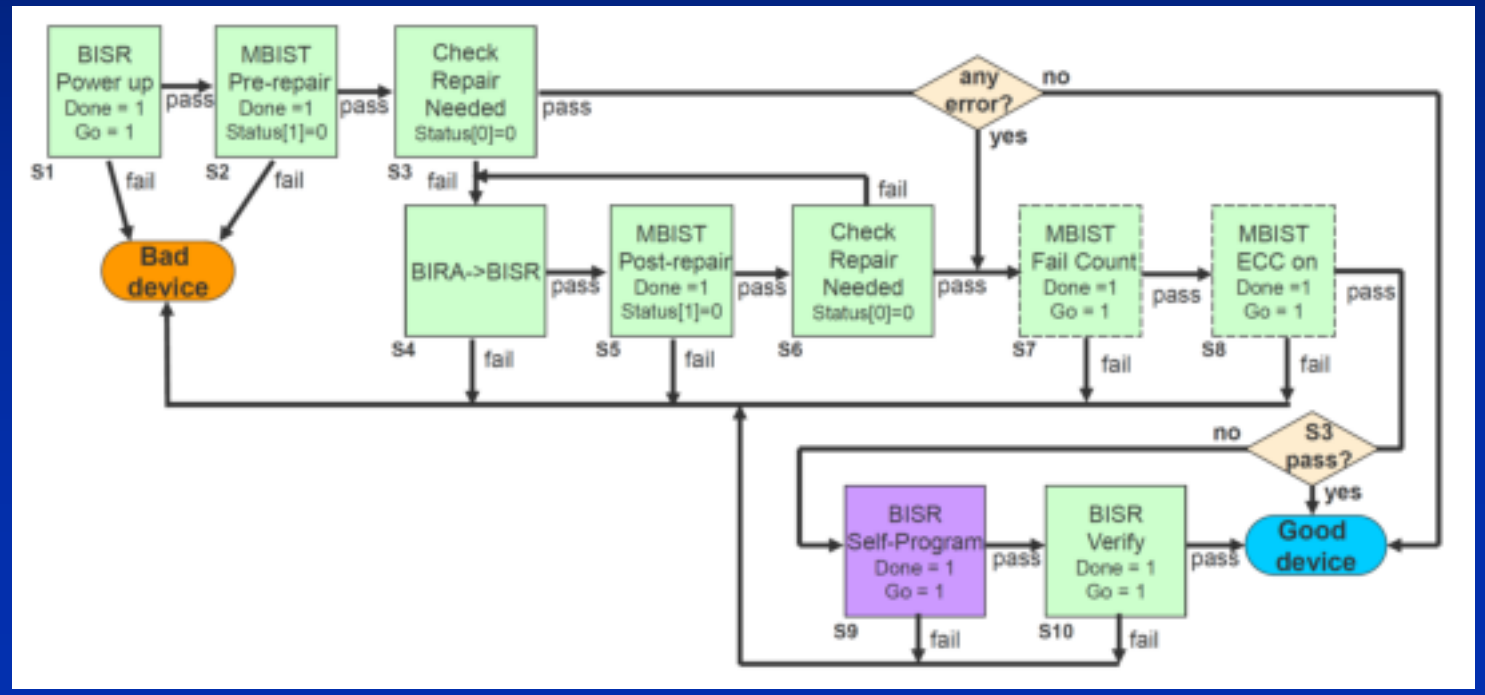
- A typical scenario is to use two-bit error correction, where one ECC bit is used to repair single-bit fails during manufacturing, leaving at least one error correction capability for in-field correction

ECC-aware test and repair technology

SRAM test flow

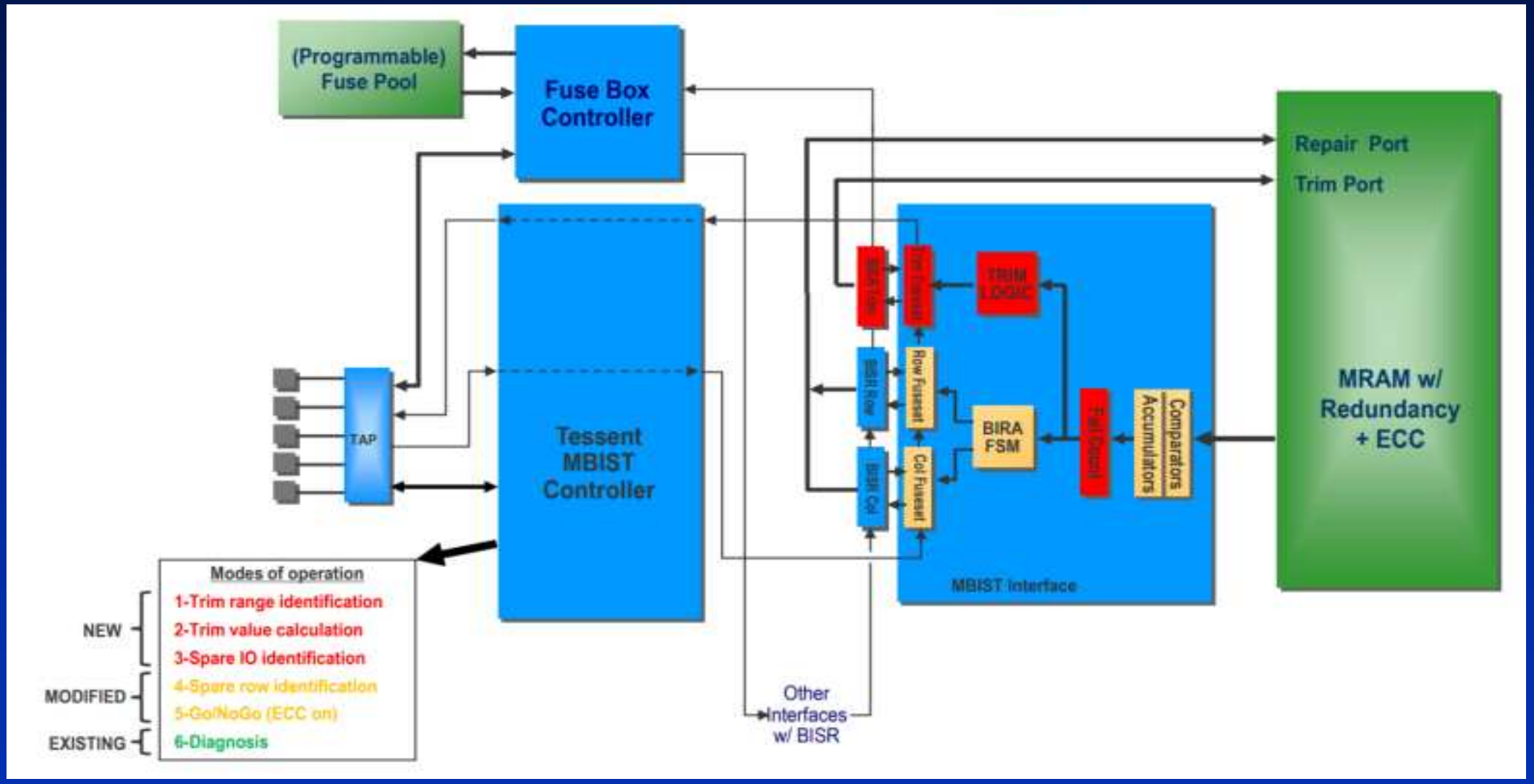


MRAM test flow (leverages SRAM test flow)



ECC-aware test and repair technology

Hardware architecture to support MRAM



How to avoid ECC test escapes

Standard MBIST: may miss multi-bit defects

Word defectivity	stuck0						stuck1	
1 error detected	0	0	0	0	0	0	0	0
1 error detected	1	1	1	1	1	1	1	1
1 error detected	0	1	0	1	0	1	0	1
1 error detected	1	0	1	0	1	0	1	0

MBIST test algorithm data pattern

0x00, 0xFF, 0x55, 0xAA

0x00, **0xFF**, 0x55, 0xAA

0x00, 0xFF, **0x55**, 0xAA

0x00, 0xFF, 0x55, **0xAA**

ECC-aware MBIST: detects multi-bit defects

Word defectivity	stuck0						stuck1	
+ 0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1

MBIST test algorithm data pattern

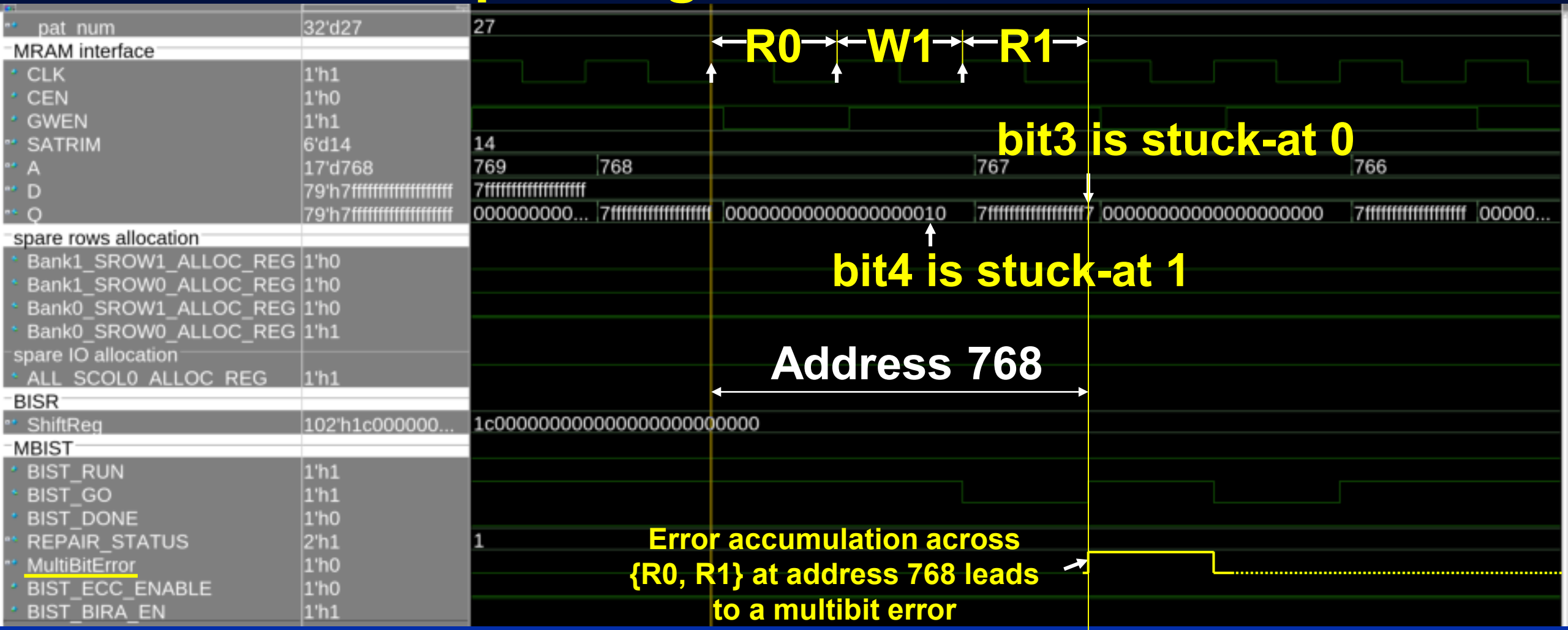
0x00, 0xFF

0x00, **0xFF**

same address

Error accumulation is a key new feature to avoid ECC test escapes

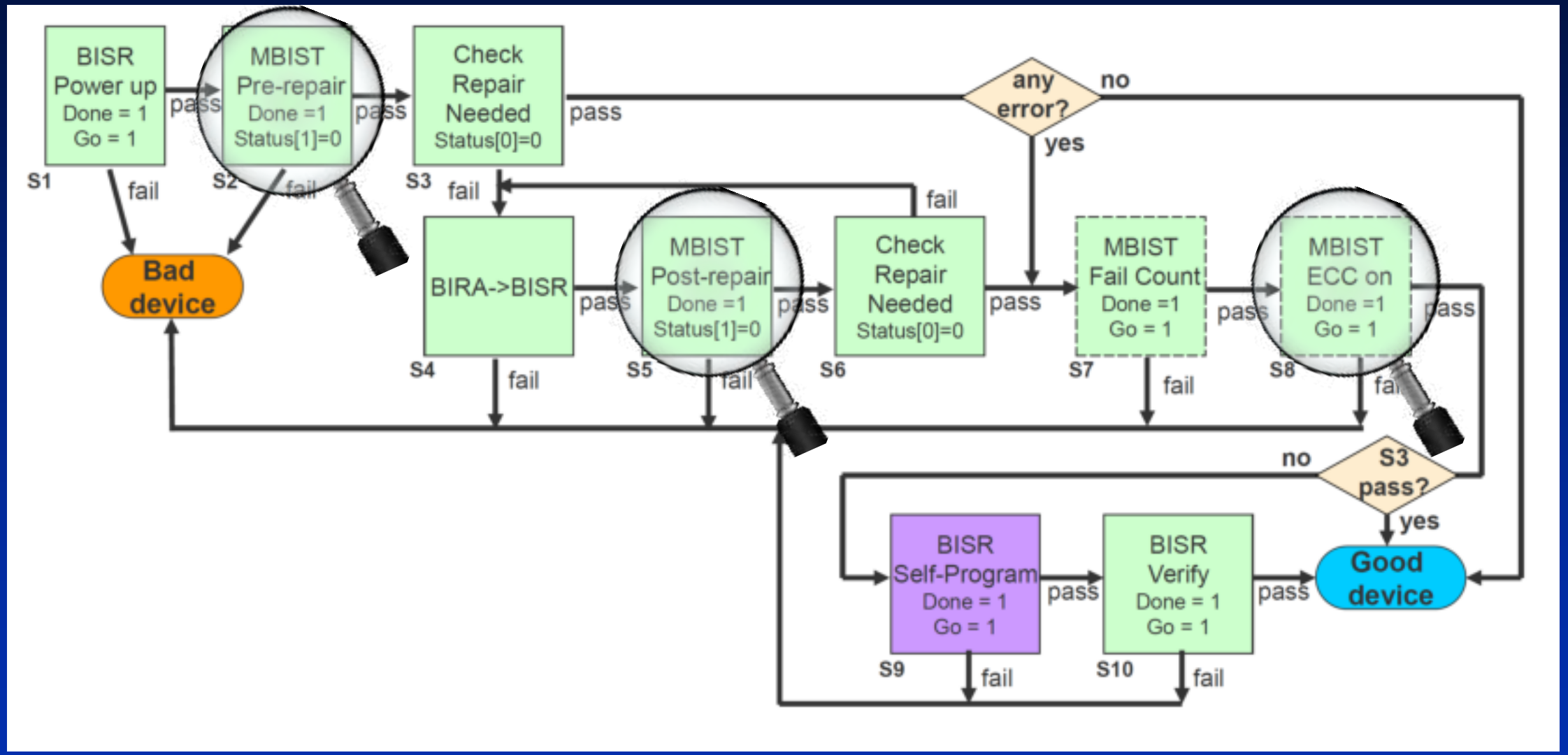
ECC test escape mitigation with error accumulation



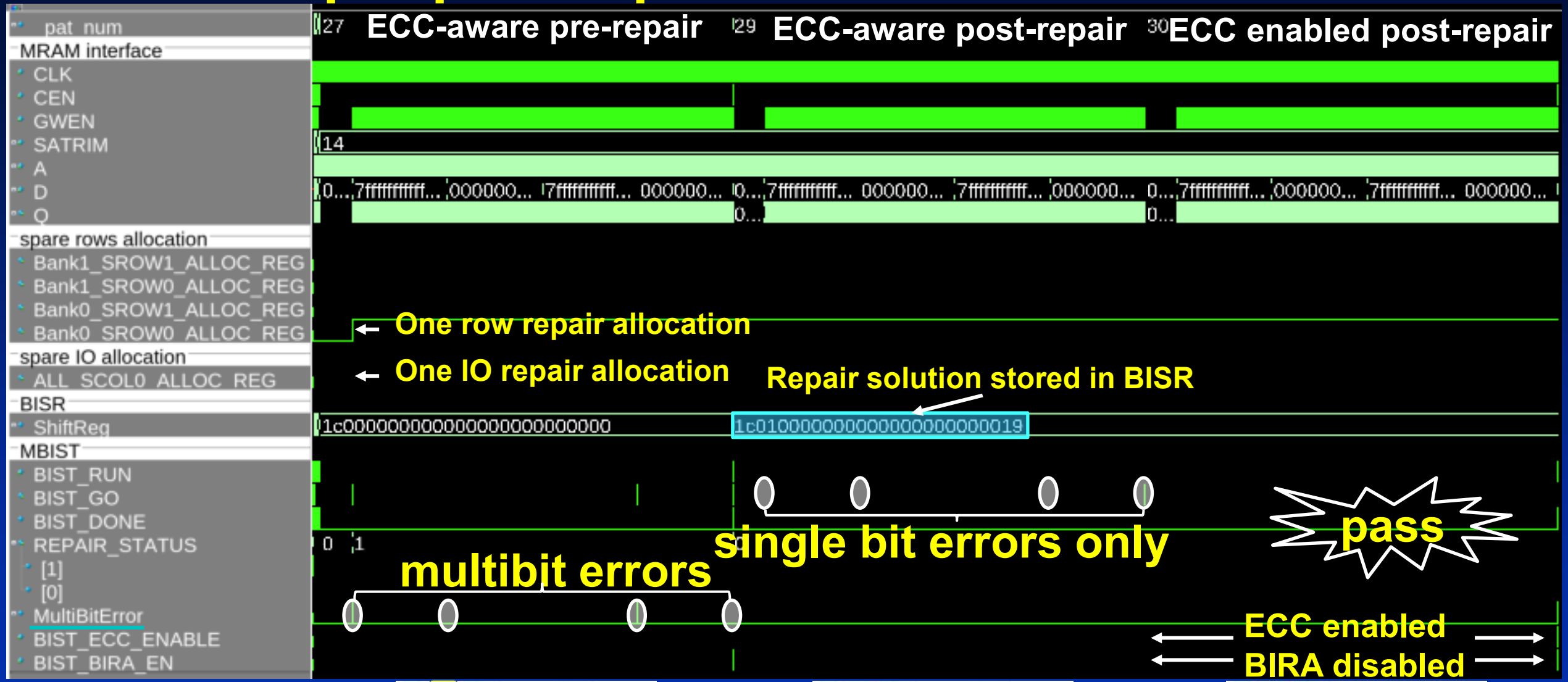
Intentional errors injection

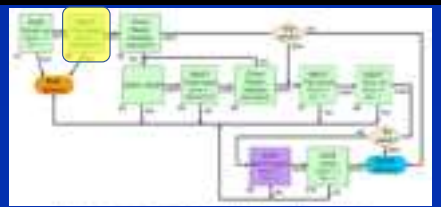
Bit position	Address	fault	Repair involved in 1bit ECC repair mode
Bit3	768	Stuck at 0	Row repair, thanks to error accumulation
Bit4		Stuck at 1	

Overview of three main tests



MBIST pre/post-repair tests





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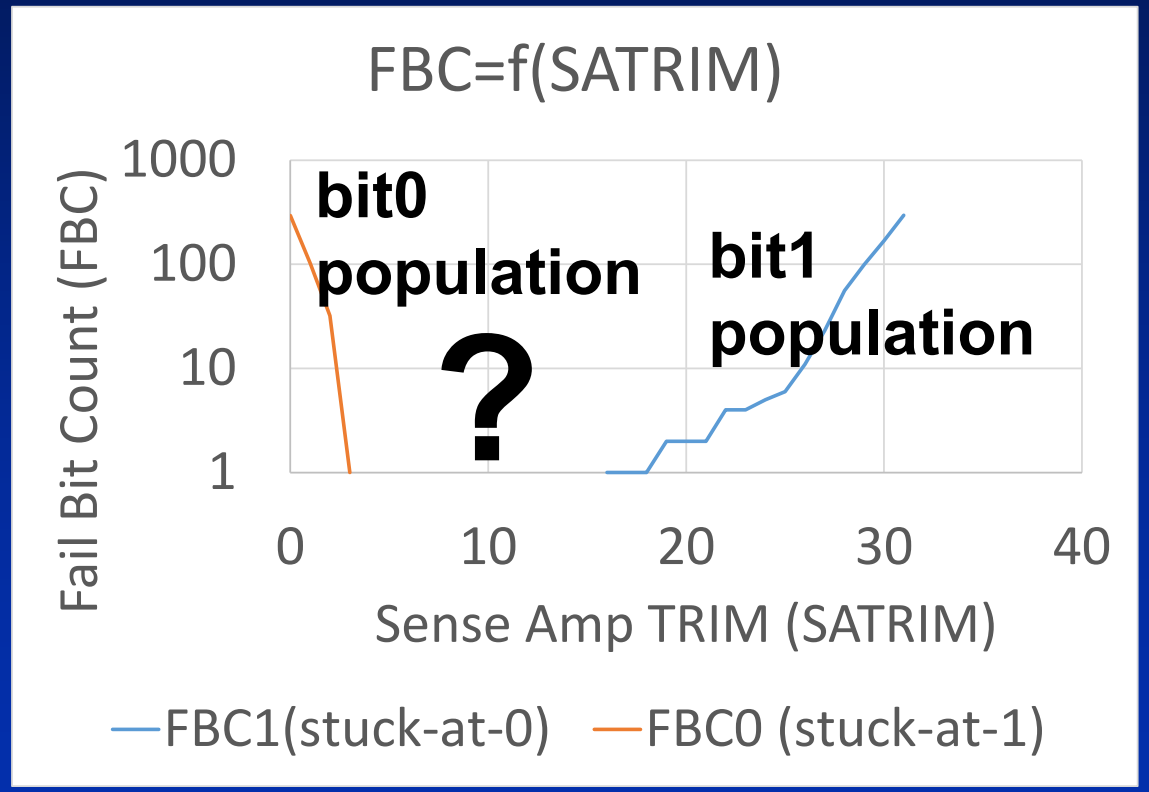
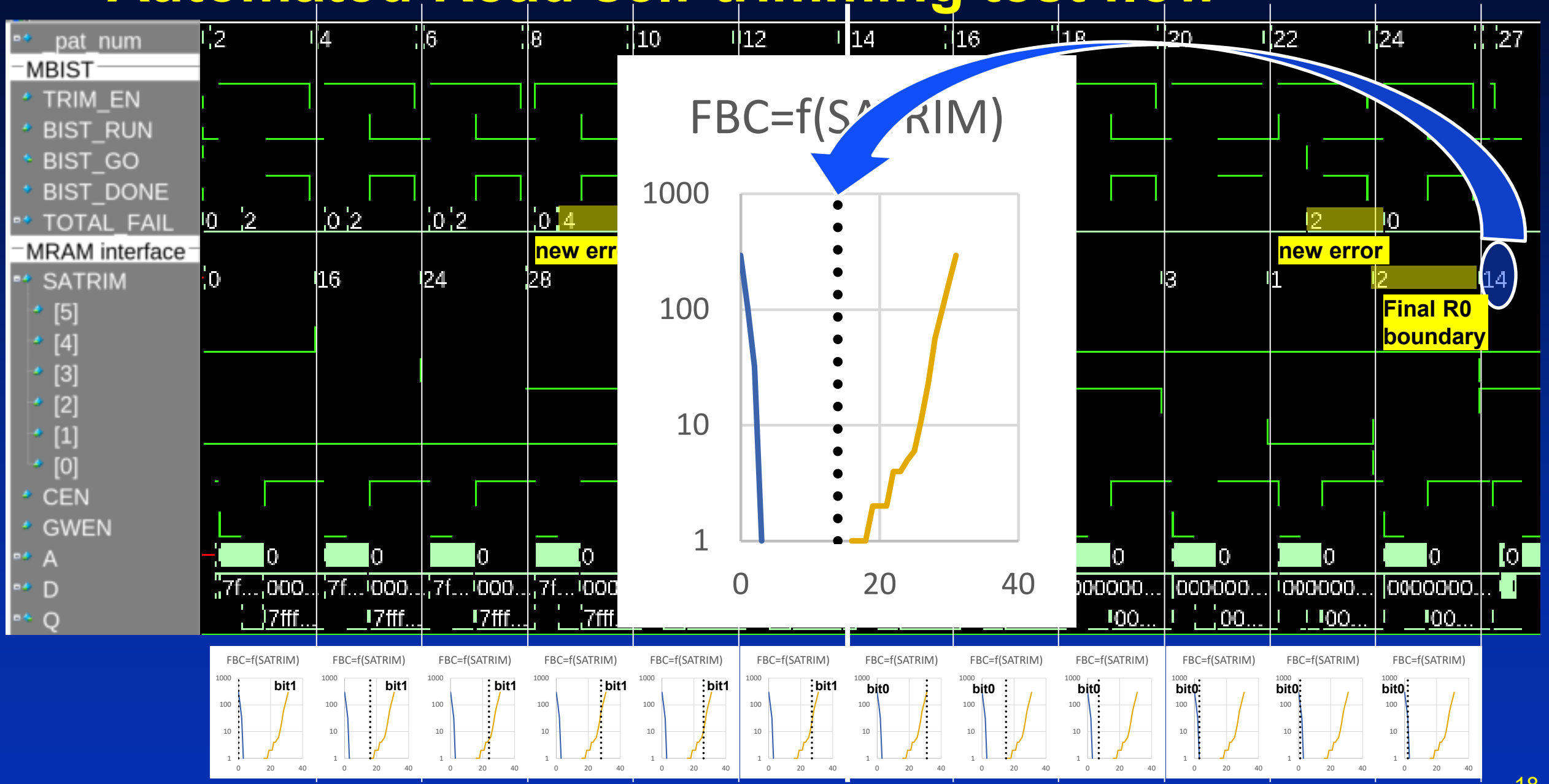
MRAM testing challenges

Memory BIST solution to enable reference trimming

- Trimming is the process of determining a reference value, which decides if the read (electrical) value must be interpreted as a logical ‘0’ or as a logical ‘1’
- For MRAM, whose storage elements are resistance-based, trimming is done to determine a specific reference resistance
- This reference value cannot be determined up-front with high confidence but must be learned, preferably on-chip by using fully autonomous circuitry for each memory and sense amplifier



Automated Read self-trimming test flow



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Summary and Conclusion

- We demonstrated the effectiveness of the automated ECC-aware test and repair technology
  - The same technology is applicable to all types of RAM
- The technology allows us to trade-off simple error correction using ECC versus using repair resources during manufacturing test
- Performing online/offline MBIST testing to detect errors before they become uncorrectable enables us to secure yield on our most advanced technology nodes